IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPELLANT:	Dee Gardiner
SERIAL NO.:	09/694,411
FILED:	October 23, 2000
CONFRM. NO.:	9053
FOR:	METHOD FOR REDUCING TRANSPORT DELAY IN AN IMAGE GENERATOR
ART UNIT:	2628
EXAMINER:	Roberta D. Prendergast
DOCKET NO:	2469-T9180

CERTIFICATE OF DEPOSIT

DATE OF DEPOSIT: December 3, 2007

I hereby certify that this paper or fee (along with any paper or fee referred to as being attached or enclosed) is being electronically deposited using EFS Web with the United States Patent Office on the date indicated above.

/Steve M. Perry/

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APPELLANTS' REPLY BRIEF UNDER 37 C.F.R. § 41.41

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
Mail Stop Appeal Brief – Patents

Sir:

Appellants submit this Reply Brief in response to the Examiner's Answer mailed on October 3, 2007 in connection with their appeal from the final rejection of the Patent Office, sent on August 27, 2007, in the above-identified application. This Reply Brief is being filed pursuant to 37 CFR 1.193(b) within two months of the date of the Examiner's Answer.

STATUS OF CLAIMS

Claims 10-14, 24, 26-29, 32 and 34-35 remain pending. Claims 1-9, 15-23, 25, 30, 31, 33, and 36-38 have been previously canceled. Claims 10-14, 24, 26-29, 32 and 34-35 stand rejected. The claims on appeal in this application are 10-14, 24, 26-29, 32 and 34-35.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The issues presented for review are:

a. whether independent claim 10 and dependent claims 11 and 13 are unpatentable under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 5,864,342 (hereinafter "Kajiya");

b. whether dependent claims 12 and 14 are unpatentable under 35 U.S.C. § 103(a) as being obvious over Kajiya in view of U.S. Patent No. 6,853,381 (hereinafter "Grigor").

c. whether independent claims 24 and 32 and dependent claims 26-29, 32, 34 and 35 are unpatentable under 35 U.S.C. § 103(a) as being obvious over Kajiya in view of U.S. Patent No. 6,316,974 (hereinafter "Taraci");

ARGUMENT

A. Examiner's Answer

In the Examiner's Reply Brief mailed on October 3, 2007, the Examiner has asserted a new section of the Kajiya reference as supporting the argument that Kajiya teaches the use of a single pixel frame buffer for simultaneous rendering and display of computer generated graphical information, as recited in independent claims 10, 24 and 32. Specifically, the Examiner asserts that Column 16, lines 15-25 of Kajiya teaches "wherein the tiler uses a single common buffer with a free list to represent free memory in the common buffer that is allocated as new fragment record are generated and added to when fragment records are resolved." (Sec. 10, Response to Argument, Examiner's Reply Brief, Page 10, bottom paragraph).

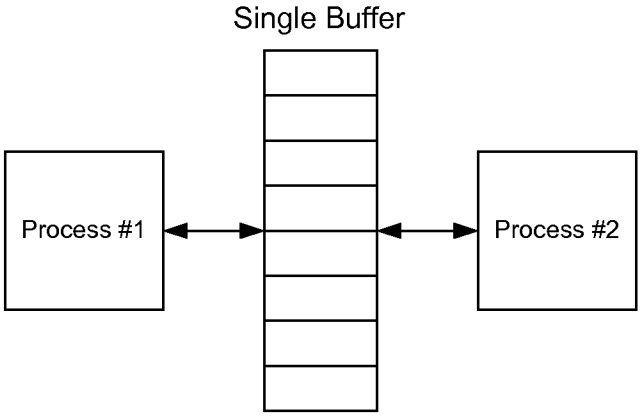
This reference was not specifically addressed in the Appeals Brief. An explanation of this citation is given below to provide a better understanding of the technology disclosed in Kajiya.

B. The Kajiya Reference

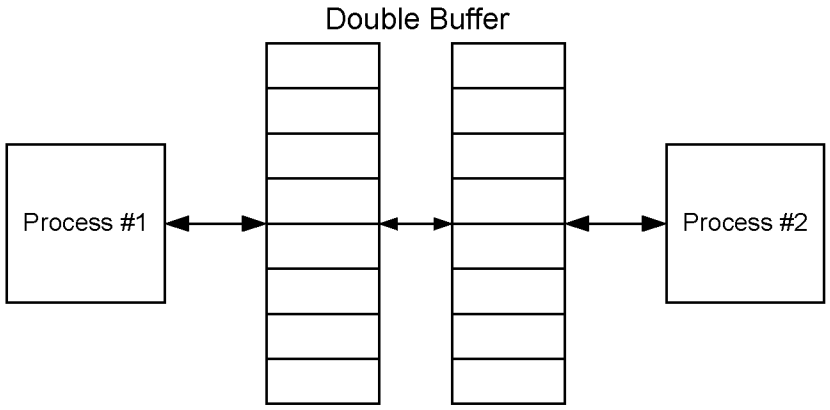
Col. 16, lines 15-25 of the Kajiya reference discloses two methods for resolving anti-aliasing data for the pixels after the tiling of the polygons in a chunk. In one embodiment, the tiler uses double buffering to resolve a previous chunk while the next is tiled. An alternative method is also disclosed, in which the tiler uses a "common buffer with a free list". The free list represents free memory in the common buffer that is allocated as new fragment records are generated and added to when fragment records are resolved. (Col. 16, lines 15-25).

The Examiner is confusing the concepts of single and double buffering with the separate idea of using either one or two memories. A "common buffer" is not defined

within the Kajiya specification. However, one of skill in the art would understand the term "common buffer", as used in Kajiya to be a memory device used to store information. The use of a common buffer (memory storage device) is not the same as a standard single buffer. For a single buffer there are typically two or more processes that are accessing the same block of memory, as illustrated below:

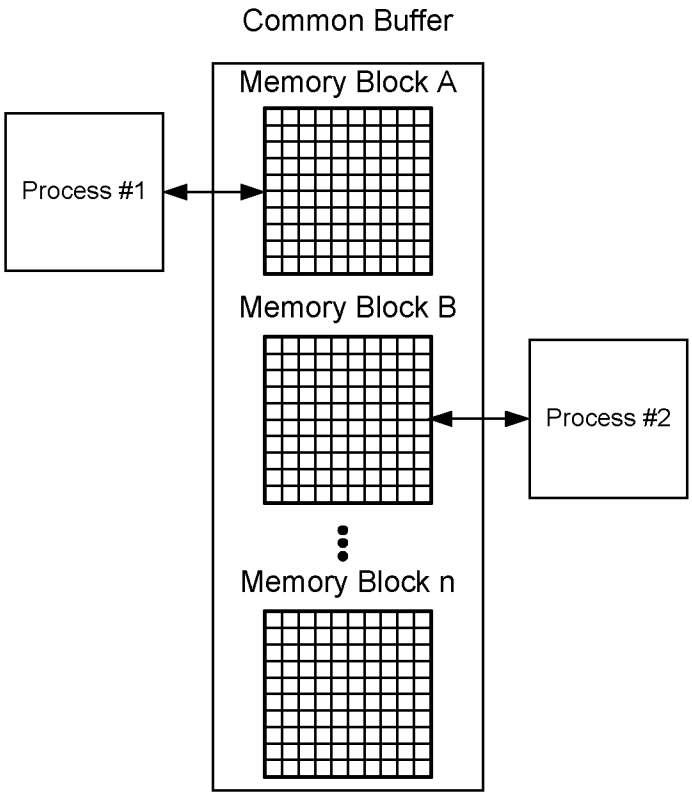


The two processes typically access the single buffer memory block sequentially, wherein process #1 writes to the block and then process #2 reads from the block, or vice versa.

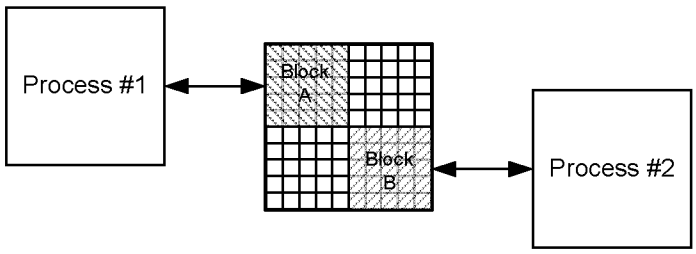


In a double buffer, as illustrated above, each process has an independent chunk of memory allocated to it. Process #1 does not access the block allocated to process #2 and vice versa. This may or may not be true with a "memory" device.

A common buffer may be comprised of multiple memories. For example, processes accessing a common buffer may be illustrated as:



Memories A and B can be swapped to hand data between the two processes. This works similarly to double buffered memory. A common buffer comprising a single memory can be diagramed as:



Block A and Block B are blocks of space within a single memory. The address pointers for blocks A and B can be swapped to hand data between the two processes. Double or even triple buffering within a single memory is very common for software

programs. The hardware may only include one memory coupled to a CPU, so multiple buffers are implemented as needed within the single memory.

C. Appellant's Argument

The Kajiya reference states in column 6, lines 23-34 that "[u]sing a common depth or rasterization buffer saves memory." One skilled in the art may interpret this statement as using a single memory instead of two separate memories. However, in lines 16-19 of column 6, an example is diagramed in which "all of the geometry for a first chunk can be rasterized into a single rasterization buffer ***before*** geometry for the next chunk is rasterized to the same rasterization buffer." This may be referencing a single memory, but it is **referring to two independent processes in time**. **Two different processes in time accessing the same memory is one definition of double buffering**. The first operation is performed ***before*** the second operation. This is double buffering within a single memory.

Thus, it can be seen that while Kajiya may reference a single, "common buffer" memory, that memory is still being used as a double buffer. This act of double buffering would not result in the present invention of using a single pixel frame buffer to simultaneous render and display computer generated graphical information, as recited in the claims of the present invention.

Additionally, even if the common buffer recited in Kajiya were used as a single buffer, the invention disclosed in Kajiya does not result in the present invention. Specifically, Kajiya discloses that after the tiler is used to resolve the anti-aliasing data for the pixels, an image processor compresses the resolved chunk using a compression scheme. (See col. 16, lines 25-30). As the image processor resolves a block of pixels, it can compress another block. The image processor then stores the

compressed chunk in a shared memory. The compressed chunks in the shared memory then go through a series of processes involved in the gsprite engine where warping using affine transformations occurs.

In contrast, claim 10 of the present invention recites the steps of:

(c) rendering 144 the screen bins 152 by row from top to bottom, into the single pixel frame buffer (page 11, lines 3-5);

(d) displaying 142 at least one row of screen bins 152 rendered before the rendering of all the screen bins has completed, wherein the displaying of the screen bins 152 takes place after a selected portion of the screen bins for a current field have been rendered. (page 10, lines 5-11).

The buffer disclosed in col. 16, lines 15-25 cannot be used to render screen bins into a single pixel frame buffer and then display at least one row of screen bins rendered before the rendering of all the screen bins has completed, as recited in steps (c) and (d) above. Rather, all of the compressed chunks are sent to a shared memory. The images are then read from the shared memory, transformed to physical output device coordinates by the gsprite engine, composited in the compositing buffer, transferred to a DAC, and then transferred to an output device. (See Kajiya, Col. 16, lines 30-36). These additional steps make it impossible for the double buffer or common buffer disclosed in Kajiya to accomplish the step (d) above of displaying at least one row of screen bins rendered before the rendering of all the screen bins has completed. Independent claims 24 and 32 also both include the limitation of rendering screen bins into a single pixel frame buffer to enable simultaneous rendering and display.

Therefore, in view of the information above, Appellants respectfully submit that independent claims 10, 24 and 32 present patentable subject matter, and that the rejection of these claims should be overturned.

The remaining arguments detailed in the Examiner's Answer are adequately discussed in the Appellants' Appeal Brief.

CONCLUSION

Appellants respectfully submit that the claims on appeal set forth in the Appendix of Appellants' Appeal Brief are patentably distinct from the asserted prior art references. Particularly, none of the asserted references or combinations of references motivates, teaches, or suggests one of ordinary skill in the art within the meaning of 35 U.S.C. § 102(b) or 35 U.S.C. § 103(a) to arrive at the presently claimed invention. Appellants contend that neither Kajiya alone nor Kajiya in combination with Taraci and/or Grigor teach each and every element of the claimed invention, and furthermore that they provide no reason to combine them.

For these reasons, Appellants respectfully request that the Board of Appeals reverse the rejection and remand the case to the Examiner for allowance.

No fee is required for filing of this Reply Brief.

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Dated this 3rd day of December, 2007:

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